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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,478	12/10/2003	Sung Gyu Pyo	P69370US0	5415

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,478	PYO, SUNG GYU	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/16/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgement is made of papers filed claiming priority from Korean Patent Application Nos. 2003-49462 and 2003-494463 filed on July 18, 2003 , the priority is accepted and the papers made of record in the file.

Information Disclosure Statement

The IDS filed on March 16, 2005 has been considered. The PTO-1449 has been initialed and the contract staff instructed to include a copy of the same along with the instant Office Action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17, 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrar (U.S. Patent No. 6,025,261, herein after Farrar) in view of Goldstein (U.S. Patent No. 6,277,740, herein after Goldstein).

With respect to claims 1 and 14 Farrar describes a method for forming an inductor in a semiconductor device, comprising the steps of :forming a first photoresist film on a semiconductor substrate in which a given structure is formed (Farrar figs.1A, 2 col. 1 lines patterning conductor 109/209 which includes depositing photo resist and

patterning), and then patterning the first photoresist film so that a given region of the semiconductor substrate is exposed (fig. 2, 204 is exposed);

Farrar describes depositing of Copper by spin on method but does not specifically mention its Cooper particles being nano-scale.

However , Goldstein a patent from the same filed of endeavor describes in col.7 lnes 60-65, etc. describes depositing copper by means of a spin-on method using a olution containing nano-scale copper particles to provide miniaturized building blocks, which enables quality improvement and differentiation of product characteristics at scales that may be presently achievable by commercially available micron-sized powders and smaller dimension interconnects of higher conductivity materials.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Goldstein's nano-scale cooper particles or precursors instead of Farrar's unspecified copper particles/precursors (cl. 14) in Farrar's method. The motivation to include the combination is to provide miniaturized building blocks, which enables quality improvement and differentiation of product characteristics at scales that may be presently achievable by commercially available micron-sized powders and smaller dimension interconnects of higher conductivity materials. (Goldstein col.1 lines 20-22, etc.).

The remaining limitations of claim 1/14 are :

performing a baking process (Goldstein example 5 col.7 lines 60-65), and then performing an annealing process to form a first copper layer in the patterned first photoresist film (Goldstein cls. 21,35) ; forming a second photoresist film on the entire

structure (Farrarfig. 2b 207) , and then patteming the second photoresist film to expose given portions of the first photoresist film and the first copper layer(Farrar fig.s 2b to 3, etc. via at extreme left); depositing copper by means of the spin-on method using the solution containing the nano-scale copper particles/precursor (Goldstein col.5 lines 35-40, performing a baking process, and then performing an annealing process to form a second copper layer between the patterned second photoresist films (Farrar formation of 207) ; and removing the first and second photoresist films. (Farrar figs.)

With respect to claim 2 Farrar describes the method as claimed in claim 1, wherein the nano-scale copper particles are formed with a size in the range of lnm to 20nm. (Goldstein col.4 line 14 , cl. 22, etc.)

With respect to claims 3 –6,8,9 Farrar describes the method as claimed in claim 1, wherein the solution containing the nano-scale copper particles is deposited at a temperature in the range of - 10 C to 100 C (Goldstein col. 4 lines 60-65) with a rate in the range of 100rpm to 5000rpm. a single step (1-10 times) or a multi-stage step or sin curve at a temperature in the range of 200 C to 500 C under a hydrogen atmosphere (Goldstein col. 5 lines 36-38, Ex.5), single step includes performing a baking process at any one temperature in the range of 200 OC to 500 C for 1 second to 10 minutes (see above) ,multi-stage step includes performing a baking process at several temperatures in the range of 200 C to 500 C for 1 second to 10 minutes while a pressure of 0.1 to 100Mpa is applied. (col. 6 lines 1-15).

With respect to claims 7, 10 ,11 Farrar describes the method as claimed in claim 4, wherein in case where the upon the baking process contains hydrogen only (Golstein Ex. 5) , a hydrogen atmosphere hydrogen-mixed gas such as hydrogen and argon (0 to 95%), hydrogen and nitrogen (0 to 95%) (Ex.5) , etc. a single gas and a mixed gas are used. a process of using a single hydrogen gas or a mixed gas such as .hydrogen, argon, helium, etc. and finally using a hydrogen gas, is repeated once to ten times.(see Goldstein Exs.)

With respect to claim 12 Farrar describes the method as claimed in claim 1, further comprising performing an annealing process before the first and second photoresist films are removed. (Goldstein Exs.)

With respect to claim 13 describes the method as claimed in claim 12, wherein the annealing process is performed at a temperature in the range of 50 C to 500 OC for 1 minute to 5 hours and under a hydrogen, argon, nitrogen or forming gas atmosphere.(rejected for reasons set out under claims 3-6,89 and 7,10 and 11).

With respect to claim 15 describes a method for forming an inductor in a semiconductor device, comprising the steps of: forming a first photoresist film on a semiconductor substrate in which a given structure is formed, and then patterning the first photoresist film so that a given region of the semiconductor substrate is exposed; depositing aluminum by means of a spin-on method using nano-scale aluminum particles or aluminum precursors, performing a baking process, and then performing an annealing process to form a first aluminum layer in the patterned first photoresist film; on the entire structure, and then patterning the second photoresist film to expose given

portions of the first photoresist film and the first aluminum layer; depositing aluminum by means of the spin-on method using the nano-scale aluminum particles or the aluminum precursors, performing a baking forming a second photoresist film process, and then performing an annealing process to form a second aluminum layer between the patterned second photoresist films; and removing the first and second photoresist films. (rejected for reasons se tout under claism 1,14 etc. Aluminum – Farrar col. 8 line 35, Goldstein col.1 lines 27-30).

With respect to claim 16 Farrar describes a method for forming an inductor in a semiconductor device, comprising the steps of : forming a first metal layer on a semiconductor substrate in which a given structure is formed, and then patterning the first metal layer so that a given region of the semiconductor substrate is exposed; forming a first copper layer on the entire structure and then polishing the first copper layer; forming a second metal layer on the entire structure, and then patterning the second metal layer to expose given regions of the first metal layer and the first copper layer; forming a second copper layer on the entire structure and then polishing the second copper layer; and then removing the first and second metal layers. (rejcted for reasons set out under claims 1/14, etc. above).

With respect to claim 17 Farrar describes the method as claimed in claim 16, wherein the first and second metal layers are formed using one of nickel (Ni), cobalt (Co), titanium (Ti), aluminum (Al), tungsten (W) and tantalum (Ta). (farrar col. 8lines 35-36, Goldstein col. 5 lines 18-22, claim 33)

With respect to claim 24 Farrar describes the method as claimed in claim 16, further comprising the step of performing an annealing process before the first and second metal layers are removed. (rejected for reasons set out under claims 1/14 above).

With respect to claim 25 Farrar describes the method as claimed in claim 24, wherein the annealing process is performed at a temperature in the range of 50 C to 500 C for 1 minute to 5 hours under a hydrogen, argon, nitrogen or forming gas atmosphere. (Golstein Exs. 3,5).

With respect to claim 26 Farrar describes a method for forming an inductor in a semiconductor device, comprising the steps of: forming a first metal layer on a semiconductor substrate in which a given structure is formed, and then pattering the first metal layer so that a given region of the semiconductor substrate is exposed; forming a first aluminum layer on the entire structure and then polishing the first aluminum layer, forming a second metal layer on the entire structure, and then patterning the second metal layer to expose given regions of the first metal layer and the first aluminum layer; forming a second aluminum layer on the entire structure and then polishing the second aluminum layer; and removing the first and second metal layers. (rejected for reasons se tout under claim 15, etc. above).

B. Claims 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrar (U.S. Patent No. 6,025,261, herein after Farrar) and Goldstein (U.S. Patent No. 6,277,740, herein after Goldstein) as applied to claims 1-17 ,e tc. above and further in view of Ahn et al. (U.S Patent No. 6,635,948, herein after Ahn).

With respect to claim 18 Farrar and Goldstein describes the method as claimed in claim 16.

Farrar and Goldstein do not specifically mention the deposition method to be electroplating .

However, Ahn a patent from the same filed of endeavor, describes in col.5 lines 60-65 describes the alternate uses of deposition or electroplating wherein first and second electroplating method or an electroless copper layers are formed using an plating method to provide a method of forming high coupling coefficient and quality inductors on semiconductor devices.

Therefore it would have been at the time of the invention to include Ahn' s alternate uses of deposition or electroplating method in Farrar and Goldstein"s method of wherein first and second electroplating method or an electroless copper layers are formed using an plating method . The motivation for the above combination is to provide a method of forming high coupling coefficient and quality inductors on semiconductor devices. (Ahn col. 1 lines 30_34).

With respect to claims 19 –23 Farrar describes the method as claimed in claim 18, wherein the electroplating method is performed using a plating solution in which an additive is not added to a solution, in which H2SO4 and CuSO4 are mixed in the ratio of 1:99 to 99:1(cl. 19)a forward DC plating method, a pulse-reverse plating method, or a pulse plating method, or a multi-stage plating step in which these methods are mixed. (cl. 20) (Ahn col.5 lines 60- col. 6 line10) while maintaining a concentration of HCl in the

range of I to 1000 ppm.(cl.21) further includes performing a process of adding a surface cleaning and activation agent copper layers are formed (cl. 22) (Ahn col. 5 lines 49-53) and wherein the first and second by means of a plating process using a plating any additive of polymer components such as a solution containing not suppressor, an accelerator, a leveler, etc. (Ahn col. 6 line 2, etc.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

March 31, 2006
~~September 13, 2005~~.

LONG PHAM
PRIMARY EXAMINER